DESIGN AND FABRICATION OF MJTCs ON QUARTZ SUBSTRATES AT NIST

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Abstract

Dry etching is employed in the fabrication of new planar, thin-film multijunction thermal converters (MJTCs) on quartz membranes and crystalline quartz chips at NIST. The use of crystalline quartz as a material for the membrane and for the chip improves the performance of the MJTC in the frequency range from 100 kHz to 100 MHz. Simulations of the ac-dc voltage transfer difference for a heater resistance of 400 Ω in the frequency range from 1 MHz to 100 MHz show a reduction in the ac-dc transfer difference of more than one order of magnitude in comparison with MJTCs fabricated on silicon chips.

Introduction

The standard planar MJTCs used as working standards at the National Institute of Standards and Technology (NIST) are fabricated on a silicon chip with a thin-film dielectric membrane [1]. A coaxial (straight) resistive heater and an array of thermocouples that sense small differences in temperature between dc and ac excitation are sputtered on the thin-film membrane. The hot junctions of the thermocouples are located along the heater and the cold junctions are on the silicon frame, which acts as a heat sink.

A new generation of planar MJTCs on quartz membranes and on quartz crystal chips has been fabricated and evaluated at the Physikalisch-Technische Bundesanstalt (PTB) [2]. The use of crystalline quartz as a material for the membrane and for the chip improves the frequency response of the MJTC in the frequency range from 100 kHz to 100 MHz and leads to reductions in uncertainties. Crystalline quartz has a smaller relative permittivity than Silicon ($\varepsilon_r \approx 4.5$ and 11.8, respectively). This reduces the capacitive coupling at the bonding pads to the heater and improves the high-frequency response [3]. The goal of the present work is to develop thin-film MJTCs on crystalline quartz chips at NIST.

Fabrication

AT- cut monocrystalline quartz wafers 76 mm in diameter and 250 μm thick were chosen as the chip material. The mask material for the initial wet etching consists of a 100 nm Au layer sputtered on a 30 nm Cr layer. The window with the membrane is anisotropically etched from the backside into the quartz crystal chip. The quartz etchant is a mixture of HF and NH_4F, at a constant temperature of 60°C in a Teflon jar. The wet etching is stopped after several hours when a membrane thickness of less than 20 μm is measured. To reduce the thickness of the membrane dry etching is used. The gas used for dry etching is CHF_3 with some O_2, at a power of 200 W. For this etchant the etching speed is about 20 nm/min. Figure 1 shows the results obtained etched for the AT-cut quartz wafer etched for 10 hours.

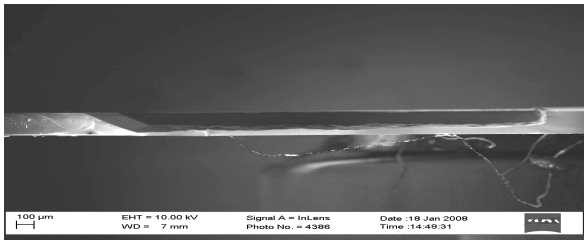

Figure 1. Scanning Electron Microscope Cross-sectional photograph of a quartz membrane.

The heater is of NiCrAlCu alloy (w_{Cr} = 0.2, w_{Al}= 0.025, w_{Cu}= 0.025) for voltage thermal converters. This alloy composition results in heaters with a low temperature coefficient of resistance of about 10 (μΩ/Ω)/°C. All devices fabricated use thermocouples of CuNi alloy (w_{Ni} = 0.45) and NiCr alloy (w_{Cr} = 0.1). The Seebeck coefficient for such a thermocouple pair is approximately 65 μV/V. Both coaxial and bifilar (∩-shaped) heater structures and the array of 100 thermocouples were fabricated using a standard photolithographic process. Wet chemical etching was used for the heater and photoresist lift-off for the thermocouples and pads. The lift-off technique is widely used for evaporated metals, and results in a reduction in processing steps.

Gold bond pads are placed at the input-output ends of the heater and at the ends of the thermocouple array. The chip is bonded to an Al_2O_3 carrier using conductive epoxy and the connections between the chip and carrier are wire bonded using thin Au wires.

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Simulation of Quartz-MJTC

To diminish the contribution to the ac-dc voltage transfer difference due to inductance, skin effect in the leads from the carrier to the input connectors of the housing and voltage standing wave in the input connectors, the Quartz-MJTC is mounted in a housing using an integrated Tee structure (Fig 2).

The model for the calculation of the ac-dc voltage transfer difference of the Quartz-MJTC using the integrated Tee, includes the ac-dc differences arising from [4]:

1. Change of the real part of the heater impedance with frequency.
2. Skin effect and inductance in the Au bonding wires.

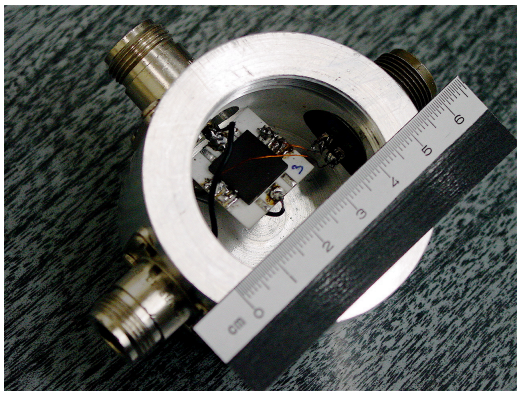
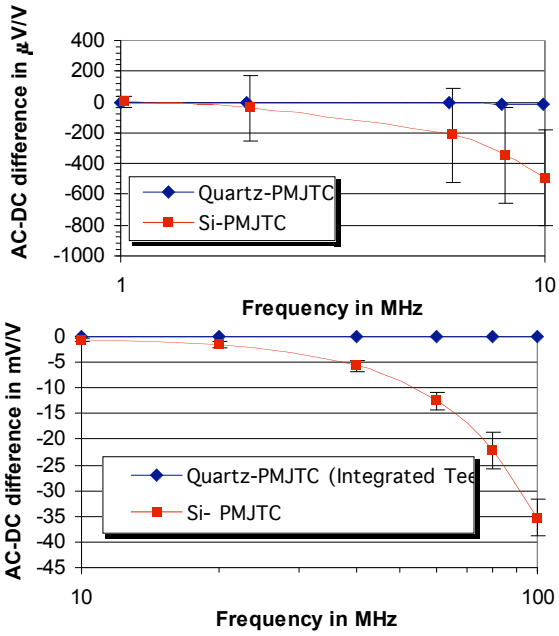


Figure 2 Housing with integrated Tee for the calculable Quartz-MJTC (top) and connector for the standard TVC (left).



Figures 3a and 3b. Measured high frequency ac-dc voltage transfer differences of Si-MJTC and calculated values of the Quartz-MJTC for a heater resistance of 400 Ω. Note scale differences.

High-Frequency AC-DC Differences

Fig. 3 (a) and (b) show a comparison between the measured ac-dc transfer differences of Si-MJTC and the calculated values of the Quartz-MJTC for a coaxial heater resistance of 400 Ω and for frequencies from 1 MHz to 100 MHz. This comparison clearly shows the advantages of crystalline quartz as a material for the membrane and the chip.

Validation of the Simulation Model

To validate the model of the Quartz-MJTC used for the simulation a comparison of the measured and calculated ac-dc transfer differences between two MJTCs with different heater resistances is realized. The input soldering pads of the ceramic carriers of two MJTCs were connected in parallel by short, thin wires. The input voltage was connected to the midpoint of these wires (Fig.4).

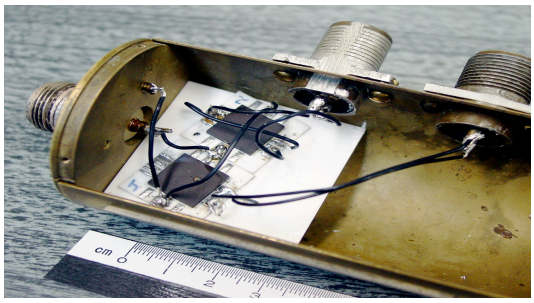


Figure 4 Two MJTCs connected in parallel in the same housing.

Conclusion

A new generation of MJTCs on crystal quartz chips and membranes are being fabricated at NIST. The results of the simulation show that the use of crystalline quartz allows significant reductions in the standard uncertainties and the ac-dc differences of the MJTCs in the frequency range from 100 kHz to 100 MHz.

References

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